INFORMAZIONI PERSONALI

Franco Fummi

✉ Franco.fummi@univr.it

Sesso M | Data di nascita 20 Agosto 1966 | Nazionalità Italiana

POSIZIONE RICOPERTA

Full Professor in Computer Architecture at the Computer Science Department of Università di Verona

ESPERIENZA PROFESSIONALE

In 1993 he was Research Assistant at the department of Computer Science of the University of Victoria (B.C.).

In 1996 he obtained the position of Assistant Professor in Computer Science at the Dipartimento di Elettronica e Informazione of Politecnico di Milano where he remained until October 1998.

In July 1998 he obtained the position of Associate Professor in Computer Architecture at the Computer Science Department of Università di Verona.

Since March 2001 he is Full Professor in Computer Architecture at the Computer Science Department of Università di Verona

He is co-founder and president of the EDA company EDALab (www.edalab.it), spin-off of the Università di Verona, focused on networked embedded systems design and tools.

Since 2012 is the head of the Department of Computer Science at the Università di Verona, that has been selected by the Italian Ministry of Education, Universities and Research (MIUR) in the 180 "Dipartimenti di Eccellenza 2018-2022" (Departments of Excellence).

ISTRUZIONE E FORMAZIONE

Franco Fummi received the Laurea degree in Electronic Engineering

at Politecnico di Milano in 1990 and the Ph.D.in Electronic and Communication Engineering in 1994 at Politecnico di Milano.

Lingua madre	Italiana		

Altre lingue

	COMPRENSIONE		PARLATO		PRODUZIONE SCRITTA
	Ascolto	Lettura	Interazione	Produzione orale	
Inglese	C2	C2	C2	C2	C2

Pubblicazioni
Progetti
Conferenze
Seminari
Riconoscimenti e premi

He has been partner in nine IST European projects: FP5-IST-2001-34607 (SYMBAD), FP6-2005-IST-5-033506 (VERTIGO), FP6-2005-IST-5-033709 (ANGEL), FP7-REGPOT-2008-1 (CREDES), FP7-2007-IST-4-247999 (COMPLEX), FP7-ICT-2011-7-288827 (SMAC), FP7-ICT-2011-7-288166 (TOUCHMORE), FP7-ICT-2013-10-611146 (CONTREX), and he coordinated the FP7-2007-IST-1-217069 (COCONUT) project.

The main research directions exploited by Franco Fummi are:

- Embedded system verification (Static verification - Dynamic verification- Semi-formal verification - Hybrid and real-time systems);

- Networked embedded systems (System/Network co-simulation - System/Network co-design - QoS-enabled design - Sensor networks and M2M systems);

- Embedded systems design (TLM-RTL synthesis and abstraction - RTL-to-SW abstraction - TLM transactor generation - Device-driver generation - Embedded SW for multicore systems - Middleware-based design).

In relation to such research areas, he published more than 300 papers; three of them received the "best paper award" respectively at IEEE EURODAC'96, IEEE DATE'99 and IEEE FDL'11.

Most relevant publications:

1. Fraccaroli, Enrico; Stefanni, Francesco; Rizzi, Romeo; Quaglia, Davide; Fummi, Franco: Network Synthesis for Distributed Embedded Systems «IEEE Transactions on Computers» , 2018, pp. 1-15

2. Lora, Michele; Vinco, Sara; Fraccaroli, Enrico; Quaglia, Davide; Fummi, Franco: Analog Models Manipulation for Effective Integration in Smart System Virtual Platforms «IEEE Transactions on CAD/ICAS» , vol. 37, n. 2, 2018, pp. 378-391

3. Vinco, Sara; Chen, Yukai; Fummi, Franco; Macii, Enrico; Poncino, Massimo: A Layered Methodology for the Simulation of Extra-Functional Properties in Smart Systems «IEEE Transactions on CAD/ICAS» vol. 36, n.10, 2017, pp. 1702-1715

4. Nicola Bombieri, Federico Busato, Franco Fummi, Pro++: A Profiling Framework for Primitive-based GPU Programming «IEEE Transactions on Emerging Topics In Computing» , 2016 , pp. 1-12

5. Sara Vinco, Valerio Guarnieri, Franco Fummi, Code Manipulation for Virtual Platform Integration «IEEE Transactions on Computers» , vol. 65, n. 9, 2016, pp. 2694-2708

6. Nicola Bombieri, Franco Fummi, Sara Vinco, A Methodology to Recover RTL IP Functionality for Automatic Generation of SW Applications «ACM Transactions on Design Automation of Electronic Systems», vol. 20, n. 3, 2015, pp. 1-25

7. Emad Ebeid, Franco Fummi, Davide Quaglia, HDL Code Generation From UML/MARTE Sequence Diagrams For Verification and Synthesis «An International Journal on Design Automation for Embedded Systems», 2015 , pp. 1-23

8. He, Diwei; Morgan, Stephen P; Trachanis, Dimitrios; van Hese, Jan; Drogoudis, Dimitris; Fummi, Franco; Stefanni, Francesco; Guarnieri, Valerio; Hayes-Gill, Barrie R A Single-Chip CMOS Pulse Oximeter with On-Chip Lock-In Detection «Sensors», vol. 15 , n. 7 , 2015 , pp. 17076-17088

9. E. Ebeid, F. Fummi, D. Quaglia, Model-Driven Design of Network Aspects of Distributed Embedded Systems «IEEE Transactions on CAD/ICAS», vol. 34 , n. 4 , 2015 , pp. 603-614

10. Nicola Bombieri, Franco Fummi, Valerio Guarnieri, Graziano Pravadelli, Francesco Stefanni, Tara Ghasempouri, Michele Lora, Giovanni Auditore, Mirella NegroMarcigaglia, Reusing RTL assertion checkers for verification of SystemC TLM models «Journal of Electronic Testing: Theory and Applications» , 2015 , pp. 1-13

11. M. Lora; R. Muradore; D. Quaglia; F. Fummi, Simulation Alternatives for the Verification of Networked Cyber-Physical Systems «Microprocessors and Microsystems» , 2015 , pp. 1-22

12. N. Bombieri; F. Fummi; V. Guarnieri; G. Pravadelli, Testbench qualification of SystemC TLM protocols through Mutation Analysis «IEEE Transactions on Computers» , vol. 63 , n. 5 , 2014 , pp. 1248-1261

13. Giuseppe Di Guglielmo, Luigi Di Guglielmo, Andreas Foltinek, Masahiro Fujita, Franco Fummi, Cristina Marconcini, Graziano Pravadelli, On the integration of model-driven design and dynamic assertion-based verification for embedded software «The Journal Of Systems And Software» , vol. 86 , 2013 , pp. 2013-2033

14. N. Bombieri, E. S. M. Ebeid, F. Fummi, M. Lora, On the Reuse of Heterogeneous IPs into SysML Models for Integration Validation «Journal of Electronic Testing: Theory and Applications» , 2013 , pp. 1-20

15. A. Acquaviva, N. Bombieri, F. Fummi, S. Vinco, Semi-Automatic Generation of Device Drivers for Rapid Embedded Platform Development «IEEE Transactions on CAD/ICAS» , vol. 32 , n. 9 , 2013 , pp. 1293-1306

16. Luigi Di Guglielmo, Franco Fummi, Graziano Pravadelli, Francesco Stefanni, Sara Vinco, UNIVERCM: The UNIversal VERsatile Computational Model for Heterogeneous System Integration «IEEE Transactions on Computers» , vol. 62 , 2013 , pp. 225-241

17. N. Bombieri, F. Fummi, V. Guarnieri, FAST: An RTL Fault Simulation Framework based on RTL-to-TLM Abstraction «Journal of Electronic Testing: Theory and Applications» , vol. 28 , n. 4 , 2012 , pp. 495-510

18. N. Bombieri, F. Fummi, V. Guarnieri, F. Stefanni, S. Vinco, HDTLib: an efficient implementation of SystemC data types for fast simulation at different abstraction levels «An International Journal on Design Automation for Embedded Systems» , vol. 16 , n. 2 , 2012 , pp. 115-135

19. Guarnieri V., Di Guglielmo G., Bombieri N., Pravadelli G., Fummi F., Hantson H., Raik J., Jenihhin M., Ubar R., On the Reuse of TLM Mutation Analysis at RTL «Journal of Electronic Testing: Theory and Applications» , vol. 28 , n. 4 , 2012 , pp. 435-448

20. Izosimov V., Di Guglielmo G., Lora M., Pravadelli G., Fummi F., Peng Z., Fujita M., Time-Constraint-Aware Optimization of Assertions in Embedded Software «Journal of Electronic Testing: Theory and Applications» , vol. 28 , n. 4 , 2012 , pp. 469-486

21. N. Bombieri, F. Fummi, G. Pravadelli, Automatic Abstraction of RTL IPs into Equivalent TLM Descriptions «IEEE Transactions on Computers» , vol. 60 , n. 12 , 2011 , pp. 1730-1743

22. Di Guglielmo Giuseppe; Di Guglielmo Luigi; Fummi Franco; Pravadelli Graziano, Efficient Generation of Stimuli for Functional Verification by Backjumping Across Extended FSMs «Journal of Electronic Testing: Theory and Applications» , vol. 27 , n. 2 , 2011 , pp. 137-162

23. N. Bombieri, M. Ferrari, F. Fummi, G. Di Guglielmo, G. Pravadelli, F. Stefanni, A. Venturelli, HIFSuite: Tools for HDL Code Conversion and Manipulation «Eurasip Journal On Embedded Systems (Print)» , vol. 2010 , n. 436328 , 2010 , pp. 1-20

24. N. Bombieri, F. Fummi, D. Quaglia, System/Network Design Space Exploration based on TLM for Networked Embedded Systems «ACM Transactions on Embedded Computing Systems» , vol. 9 , n. 4 , 2010 , pp. 37:1-37:32

25. Fummi F.; Loghi M.; Poncino M.; Pravadelli G., A Co-Simulation Methodology for HW/SW Validation and Performance Estimation «ACM Transactions on Design Automation of Electronic Systems» , vol. 14 , n. 2 , 2009 , pp. 23:1-23:32

26. N. Bombieri, F. Fummi, G. Pravadelli, Reuse and Optimization of Testbenches and Properties in a TLM-to-RTL Design Flow «ACM Transactions on Design Automation of Electronic Systems» , vol. 13 , n. 3 , 2008 , pp. 47:1-47:22

27. F. Fummi, G. Perbellini, eEPC: an EPCglobal-compliant Embedded Architecture for RFID-based Solutions «Journal Of Communications» , vol. 2 , n. 7 , 2007 , pp. 49-58

28. N. Bombieri, A. Fedeli, F. Fummi, G. Pravadelli, Hybrid Incremental Assertion-Based Verification for Functional Validation in TLM Design Flows «IEEE Design &Test of Computers» , vol. 24 , n. 2 , 2007 , pp. 140-152

29. G. Di Guglielmo, F. Fummi, C. Marconcini, G. Pravadelli, Improving High-Level and Gate-Level Testing with FATE: a Functional ATPG Traversing Unstabilized EFSMs «IET Computers & Digital Techniques» , vol. 1 , n. 3 , 2007 , pp. 187-196

30. A. Fedeli, F. Fummi, G. Pravadelli, Properties Incompleteness Evaluation by Functional Verification «IEEE Transactions on Computers» , vol. 56 , n. 4 , 2007 , pp. 528-544

31. F. Fummi, M. Loghi, G. Perbellini, M. Poncino, SystemC co-simulation for core-based embedded systems «An International Journal on Design Automation for Embedded Systems» , vol. 11 , 2007 , pp. 141-166

32. F. Fummi, G. Pravadelli, Too Few or too Many Properties? Measure it by ATPG! «Journal of Electronic Testing: Theory and Applications» , vol. 23 , n. 5 , 2007 , pp. 373-388

33. F. Fummi, C. Marconcini, G. Pravadelli, Logic-Level Mapping of High-Level Faults «INTEGRATION, the VLSI Journal» , vol. 38 , n. 3 , 2004 , pp. 467-490

34. A. Fin, F. Fummi, A Remote Methodology for Embedded Systems Design and Validation «An International Journal on Design Automation for Embedded Systems» , vol. 8 , 2003 , pp. 229-247

35. F. Ferrandi, F. Fummi, G. Pravadelli, D. Sciuto, Identification of Design Erros through Functional Testing «IEEE Transactions on Reliability» , vol. 52 , n. 4 , 2003 , pp. 400-412

36. L. Benini, D. Bertozzi, D. Bruni, N. Drago, F. Fummi, M. Poncino, SystemC Co-Simulation and Emulation of Multi-Processor Systems-on-Chip «IEEE Computer» , vol. 36 , n. 4 , 2003 , pp. 53-59

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38. F. Ferrandi, F. Fummi, D. Sciuto, Test Generation and Testability Alternatives Exploration of Critical Algorithms for Embedded Applications «IEEE Transactions on Computers» , vol. 51 , n. 2 , 2002 , pp. 200-215

39. F. Fummi, M. Boschini, X. Yu, E.M. Rudnick, Sequential Circuit Test Generation Using a Symbolic/Genetic Hybrid Approach «Journal of Electronic Testing: Theory and

Applications» , vol. 17 , 2001 , pp. 321-330

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41. G. Buonanno, F. Fummi, D. Sciuto, An Extended UIO-Based Method for Protocol Conformance Testing «Journal of Systems Architecture» , vol. 46 , 2000 , pp. 225-242

42. F. Ferrandi, F. Fummi, E. Macii, M. Poncino, D. Sciuto, Symbolic Optimization of FSM Networks Based on Redundancies Identification and Removal «IEEE Transactions on CAD/ICAS» , vol. 19 , n. 7 , 2000 , pp. 760-772

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44. F. Fummi, Sciuto D., Silvano C., Automatic Generation of Error Control Codes for Computer Applications «IEEE Transactions on VLSI Systems» , vol. 3(6) , 1998 , pp. 502-506

45. Alippi C., F. Fummi, Piuri V., Sami M., Sciuto D., Testability Analysis and Behavioral Testing of the Hopfield Neural Paradigm «IEEE Transactions on VLSI Systems» , vol. 3 , n. 6 , 1998 , pp. 507-511

46. F. Fummi, D. Sciuto, A Complete Testing Strategy Based on Interacting and Hierarchical FSMs «INTEGRATION, the VLSI Journal» , vol. 23 , 1997 , pp. 75-93

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49. G. Buonanno, F. Fummi, D. Sciuto, F. Lombardi, FsmTest: Functional Test Generator for Sequential Circuits «INTEGRATION, the VLSI Journal» , vol. 20 , 1996 , pp. 303-325

50. G. Buonanno, F. Fummi, D. Sciuto, Functional Fault Models and Gate Level Coverage for Sequential Architectures «Journal of Microelectronic System Integration» , vol. 4 , 1996 , pp. 3-16

51. Buonanno G, F. Fummi, Sciuto D., TIES: a Testability Increase Expert System for VLSI Design «Journal of Electronic Testing: Theory and Applications» , vol. 6 , 1995 , pp. 203-217

52. C. Bolchini, F. Fummi, D. Sciuto, Two-Dimensional Sequential Array Architectures: Design for Testability and Reconfiguration Issues «Journal of Microelectronic System Integration» , vol. 1 , 1993 , pp. 209-220

Dati personali   Autorizzo il trattamento dei miei dati personali ai sensi del Decreto Legislativo 30 giugno 2003, n. 196 "Codice in materia di protezione dei dati personali".